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Design of High Speed DDR3 SDRAM Controller

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ABSTRACT -
In computing, DDR3 SDRAM or double-data-rate three synchronous dynamic random access memories is a random access memory interface technology used for high bandwidth storage of the working data of a computer or other digital electronic devices. DDR3 is part of the SDRAM family of technologies and is one of the many DRAM implementations. DDR3 SDRAM is the 3rd generation of DDR memories, featuring higher performance and lower power consumption. In comparison with earlier generations, DDR1/2 SDRAM, DDR3 SDRAM is a higher density device and achieves higher bandwidth due to the further increase of the clock rate and reduction in power consumption. In this work, the DDR3SDRAM controller is designed and it can interface with Look up table based Hash CAM circuit. CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all search applications. The architecture of DDR3SDRAM controller consists of Initialization fsm Command fsm, data path , bank control ,clock counter, refresh counter, Address FIFO, command FIFO ,Wdata FIFO and R_data reg

In this paper, an advanced DDR3SDRAM controller architecture was designed and which can interface with a high performance Hash-CAM based lockup circuit. The DDR3SDRAM controller normal write, read and fast read operations are verified by simulation and DDR3SDRAM controller is synthesized.

Keywords - DRAM (Dynamic random access memory), Content-addressable memory (CAM)

I. INTRODUCTION

In electronic engineering, DDR3 SDRAM or double-data-rate three synchronous dynamic random access memories is a technology used for high bandwidth storage of the working data of a computer or other digital electronic devices.DDR3 is part of the SDRAM family of technologies and is one of the many DRAM (dynamic random access memory) implementations. DDR3 SDRAM is an improvement over its predecessor, DDR2 SDRAM.

The primary benefit of DDR3 is the ability to transfer I/O data at eight times the data rate of the memory cells it contains, thus enabling higher bus rates and higher peak rates than earlier memory technologies. However, there is no corresponding reduction in latency, which is therefore proportionally higher. In addition, the DDR3 standard allows for chip capacities of 512 megabits to 8 gigabits, effectively enabling a maximum memory module size of 16 gigabytes.

In fact, it is true: DDR3 SDRAM is a sort of third reincarnation of DDR SDRAM principles. Therefore, we have every right to compare DDR3 and DDR2 SDRAM side by side here. Moreover, this comparison will hardly take a lot of time.

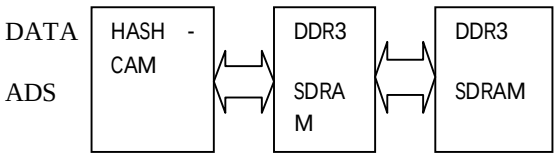
I. DDR3 SDRAM:

The frequencies of DDR3 memory could be raised beyond those of DDR2 due to doubling of the data prefetch that was moved from the info storage device to the input/output buffer. While DDR2 SDRAM uses 4-bit samples, DDR3 SDRAM uses 8-bit prefetch also known as 8n-prefetch. In other words, DDR3 SDRAM technology implies doubling of the internal bus width between the actual DRAM core and the input/output buffer. As a result, the increase in the efficient data transfer rate provided by DDR3 SDRAM doesn't require faster operation of the memory core. Only external buffers start working faster. As for the core frequency of the memory chips, it appears 8 times lower than that of the external memory bus and DDR3 buffers (this frequency was 4 times lower than that of the external bus by DDR2) So, DDR3 memory can almost immediately hit higher actual frequencies than DDR2 SDRAM, without any modifications or improvements of the semiconductor manufacturing process. However, the above described technique also has another side to it: unfortunately, it increases not only memory bandwidth, but also memory latencies. As a result, we shouldn't always expect DDR3 SDRAM to work faster than DDR2 SDRAM, even if it operates at higher frequencies than DDR2.

1.2 DDR3 Based Lookup Circuit for High-Performance Network Processing

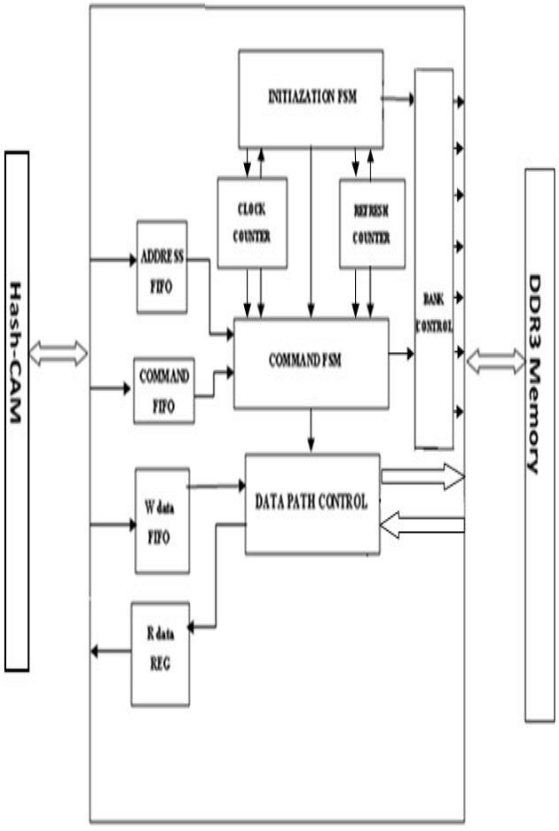
With the development of network systems, packet processing techniques are becoming more important to deal with the massive high-throughput packets of the internet. Accordingly, advances in memory architectures are required to meet the emerging bandwidth demands. Content Addressable Memory (CAM) based techniques are widely used in network equipment for fast table look up. However, in comparison to Random Access Memory (RAM) technology, CAM technology is restricted in terms of memory density, hardware cost and power dissipation. Recently, a Hash-CAM circuit , which combines the merits of the hash algorithm and the CAM function, was proposed to replace pure CAM based lookup circuits with comparable performance, higher memory density and lower cost. Most importantly, off-chip high density low-cost DDR memory technology has now become an attractive alternative for the proposed Hash-CAM based lookup circuit. However, DDR technology is optimized for burst access for cached processor platforms. As such, efficient DDR Bandwidth utilization is a major challenge for lookup functions that exhibit short and random memory access patterns. The extreme low-cost and high memory density features of the DDR technology allow a trade-off between memory utilization and memory-bandwidth utilization by customizing the memory access. This, however, requires a custom purpose DDR memory controller that is optimized to achieve the best read efficiency and highest memory bandwidth. The objective of this work was to investigate advanced DDR3 SDRAM controller architectures and derive a customized architecture for the abovementioned problem.

DDR3 SDRAM is the 3rd generation memories, featuring higher performance and lower power consumption . In comparison with earlier generations, DDR1/2 SDRAM, DDR3 SDRAM is a higher density device and achieves higher bandwidth due to the further increase of the clock rate and reduction in power consumption benefiting from *1.5V* power supply at *90 nm* fabrication technology. With *8* individual banks, DDR3 memory is more flexible to be accessed with fewer bank conflicts.



II. DESIGN OF DDR3SDRAM CONTROLLER

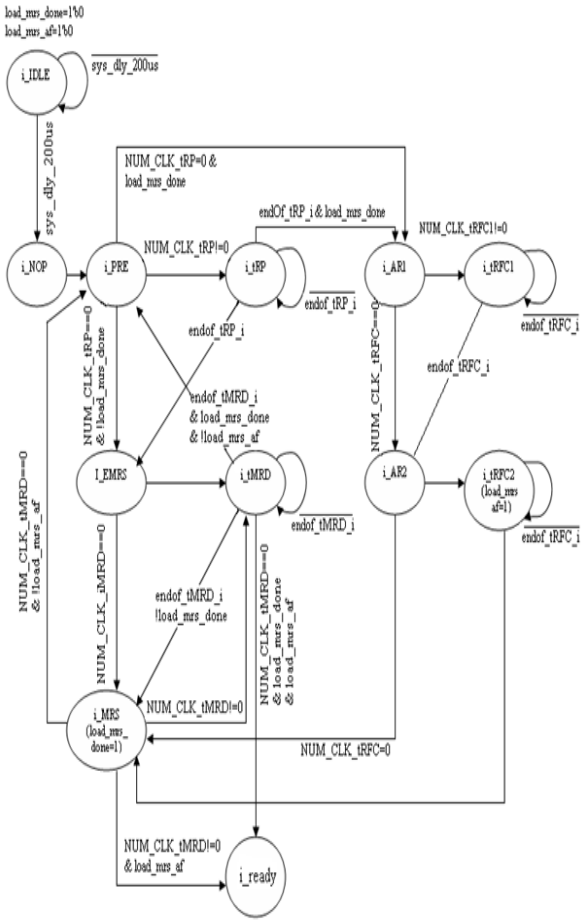
The DDR3 SDRAM uses double data rate architecture to achieve high-speed operation. The double data rate architecture is 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clockcycle data transfers at the I/O pins. The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.



The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address

signals are registered at every positive edge of CK. Input data is registered on the first rising edge of

DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble. Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed.



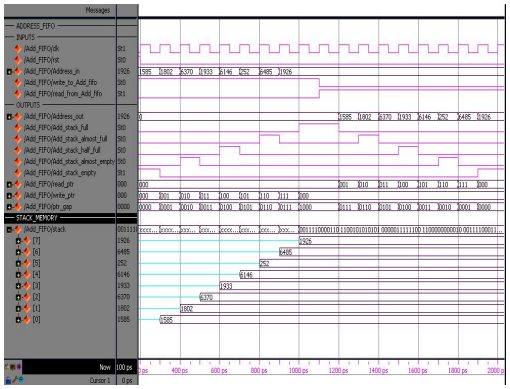
The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access. DDR3 SDRAM use READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time. A self refresh mode is provided, along with a power-saving, power-down mode.

IV. RESULTS

Address fifo

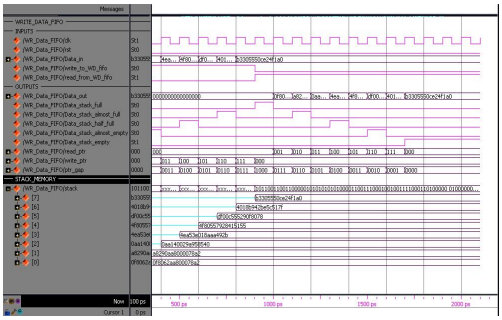
DDR3 SDRAM controller gets the address from the Address fifo so that controller can perform the read from the memory or write in to the memory address location specified by the Address fifo. Here the Address fifo width is 13 bit and stack depth is 8.



Write data fifo

DDR3 SDRAM controller gets the data from the Write data fifo in write operation in to the memory address location specified by the Address

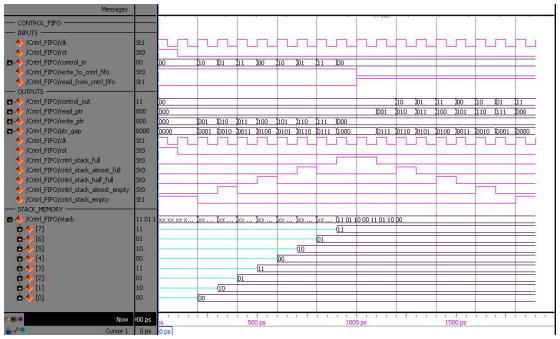
fifo. Here the Address fifo width is 64 bit and stack depth is 8.



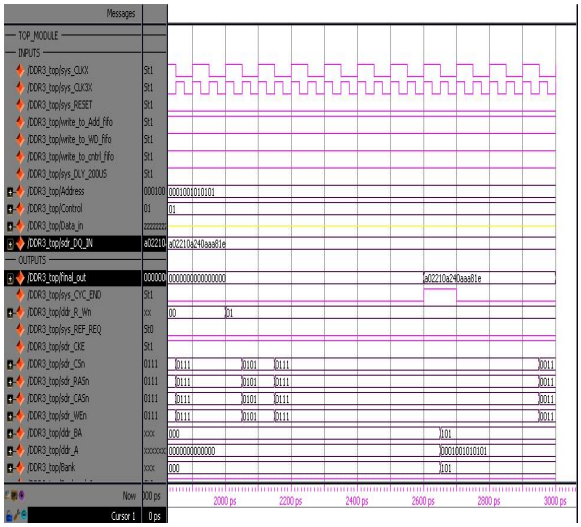
Control fifo

DDR3 SDRAM controller gets the command from the Control fifo controller can perform the read from the memory or write in to the memory address location specified by the Address fifo. Here the Control fifo width is 2 bit and stack depth is 8. If the control fifo gives the “01” DDR3 controller performs the Normal read operation. If the control is

“10” DDR3 controller performs the Normal read operation and if control is “11” DDR3 controller performs the Fast read operation.



TIMING DIAGRAMS OF READ CYCLE



ACKNOWLEDGEMENTS

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